

FIG. 1

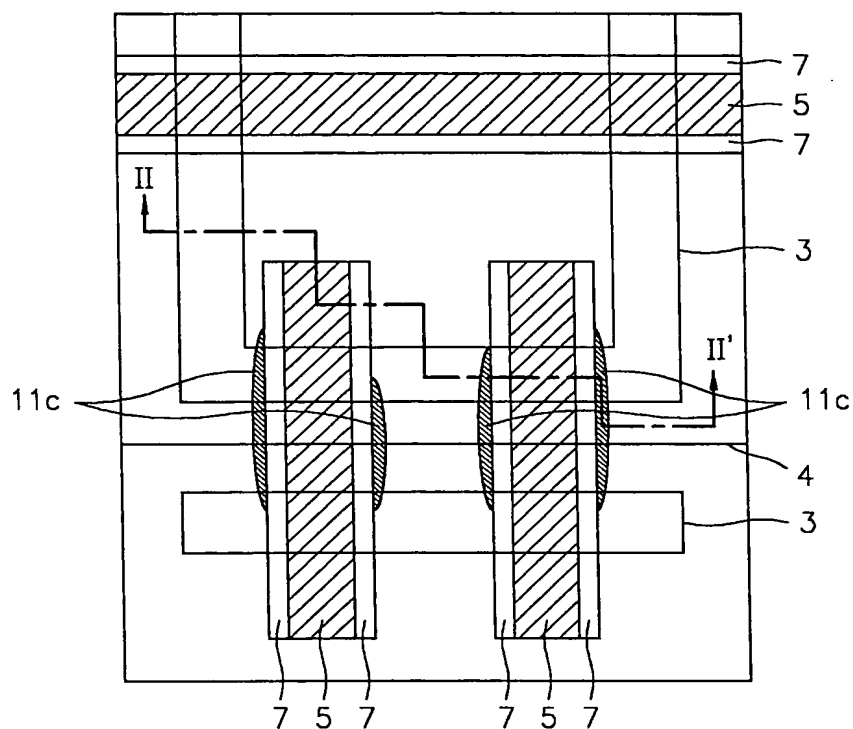


FIG. 2

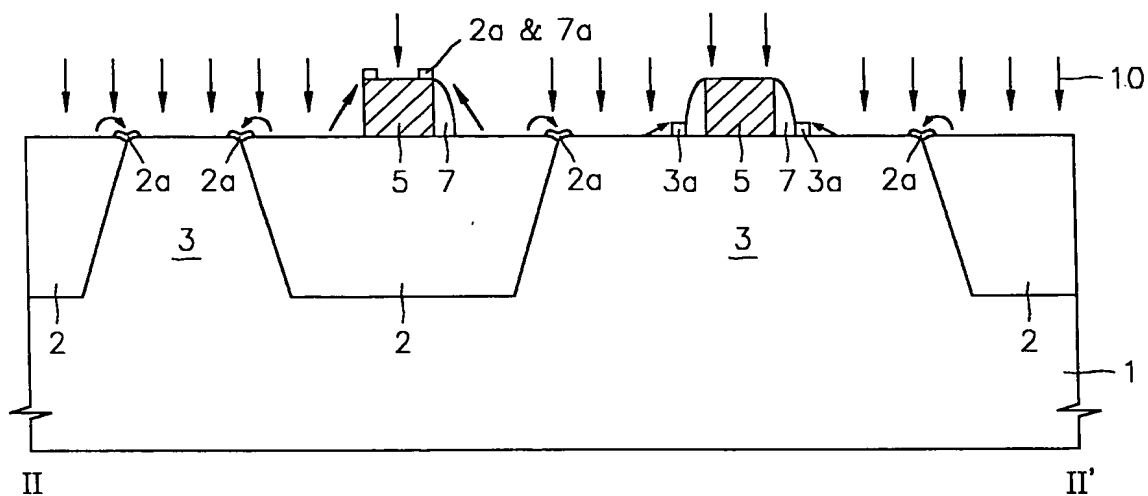


FIG. 3

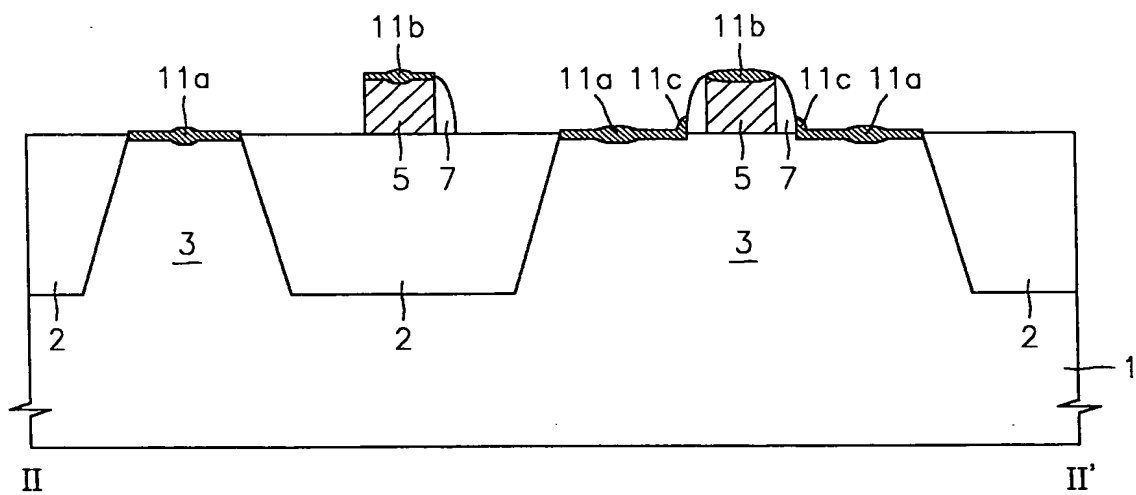
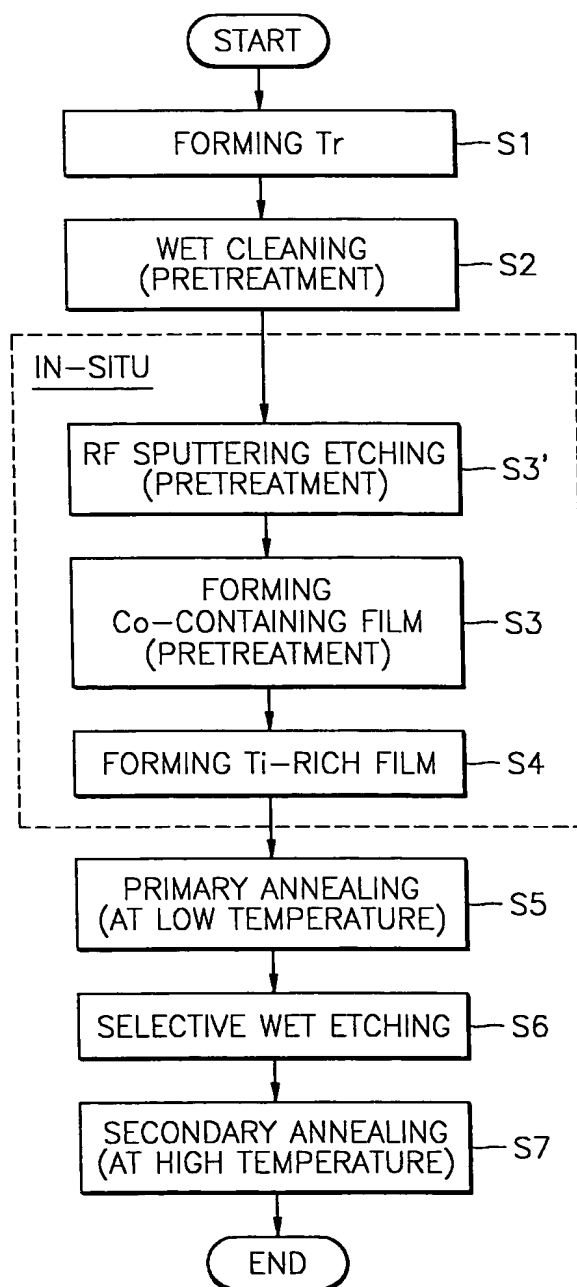




FIG. 5



A cross-sectional view of a semiconductor device. The substrate is labeled 100 and is divided into an N-WELL region and a P region. The N-WELL region contains two transistors. The first transistor has a gate stack 105 on top of a gate oxide 104, with source and drain regions 108n and 106n respectively, which are part of a larger region 109n. The second transistor has a gate stack 105 on top of a gate oxide 104, with source and drain regions 108p and 106p respectively, which are part of a larger region 109p. The P region contains a transistor with a gate stack 105 on top of a gate oxide 104, with source and drain regions 108p and 106p respectively, which are part of a larger region 109p. The regions 102 are the top surface of the substrate. The regions 107 are the side walls of the gate stacks. The regions 101 are the top surface of the substrate.

A cross-sectional view of a semiconductor device. The device is built on a substrate 100, which is divided into an N-WELL region 101 and a P region 102. The N-WELL region 101 contains two transistors. The first transistor has a gate stack 105, a gate sidewall 107, a gate bottom 104, a source/drain region 106n, and a source/drain contact 108n. The second transistor has a gate stack 105, a gate sidewall 107, a gate bottom 104, a source/drain region 106p, and a source/drain contact 108p. A dashed circle indicates a magnified view of the corner of the gate stack 105, showing a layered structure with labels 115a and 115c. The device is connected to a power supply 100.

FIG. 6C

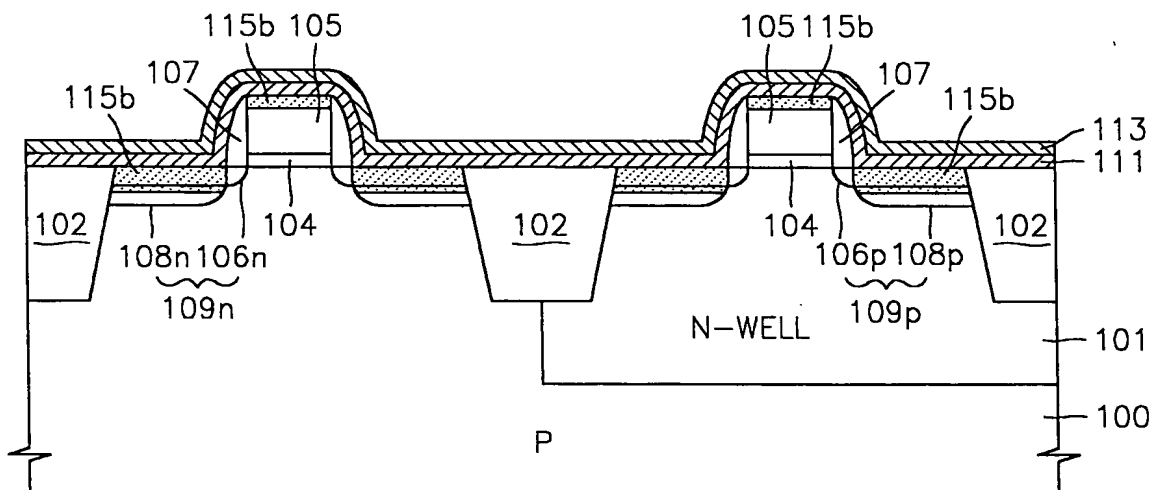


FIG. 6D

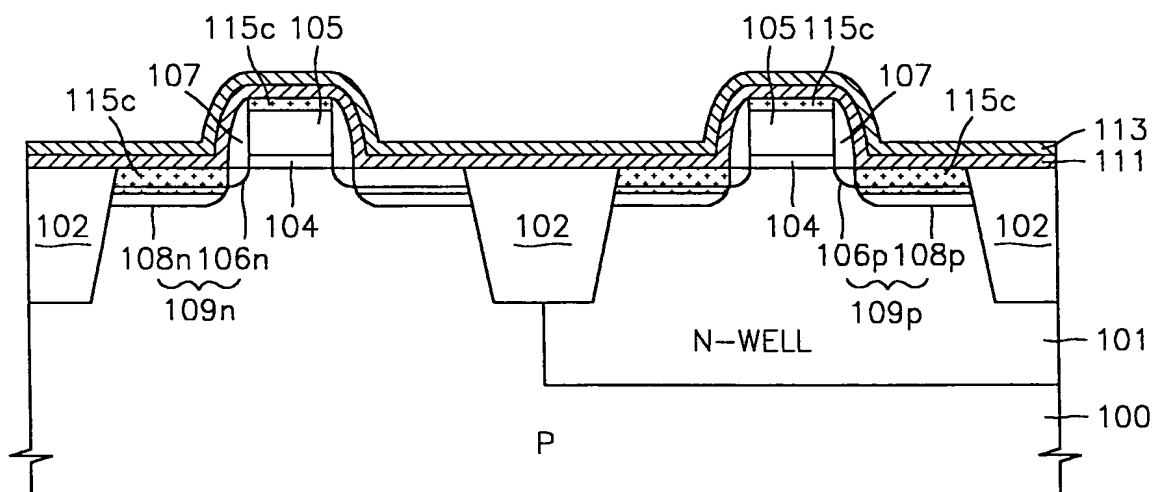


FIG. 7

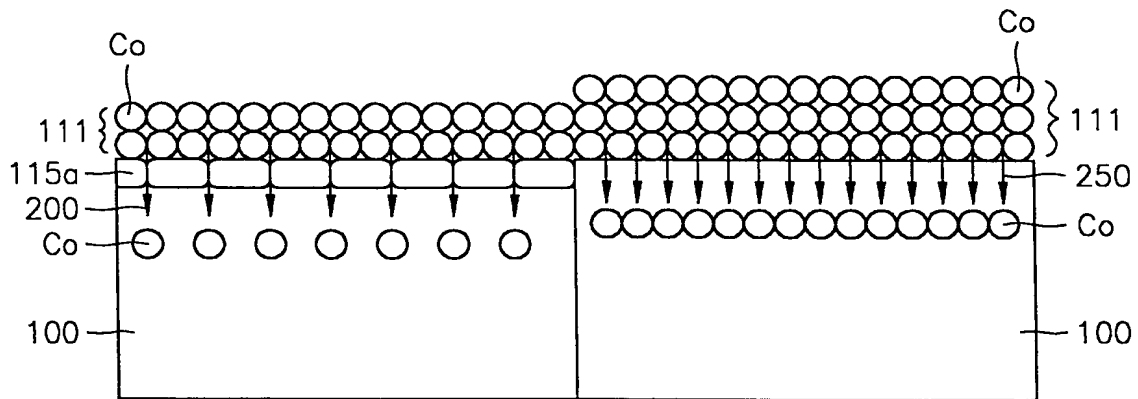


FIG. 8A

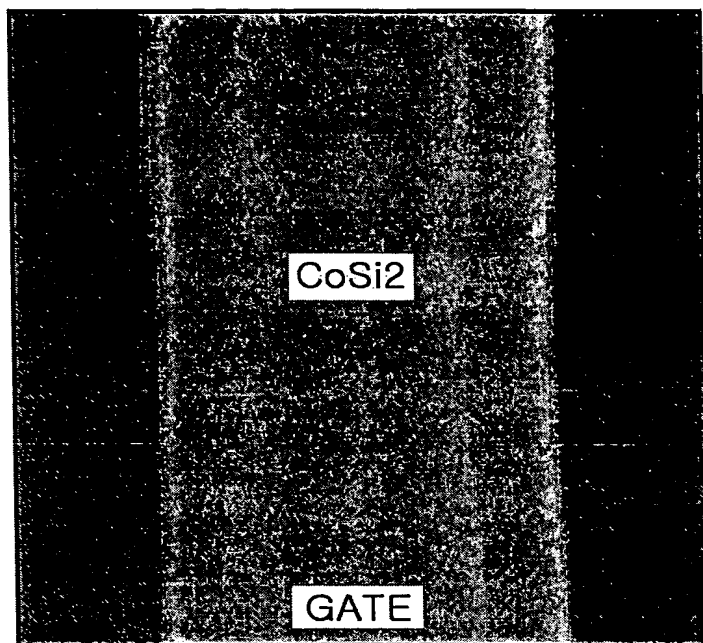
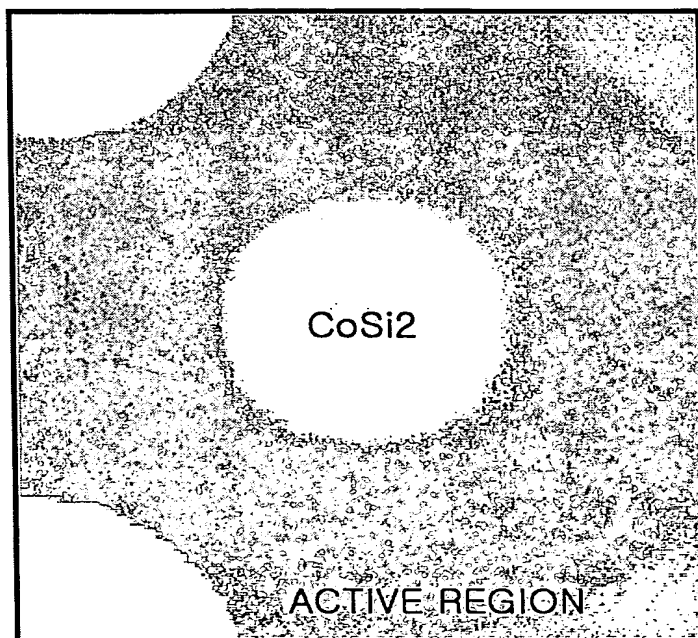


FIG. 8B





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FIG. 9A

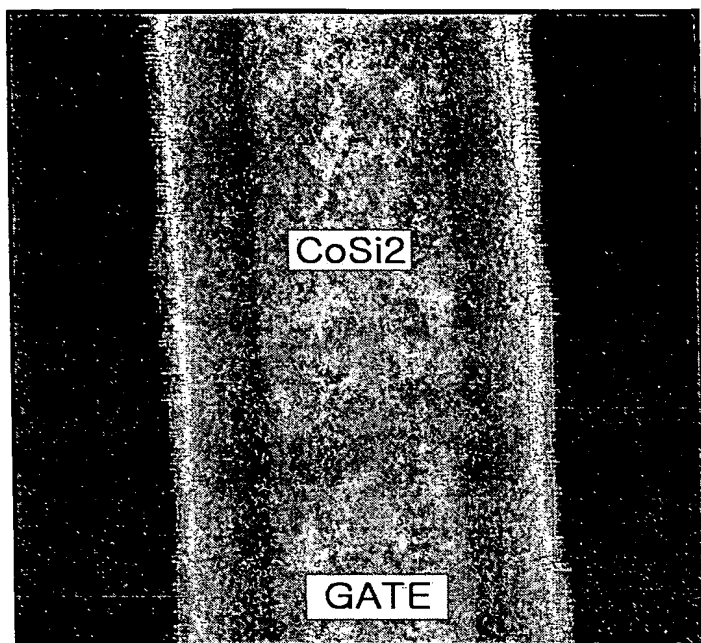
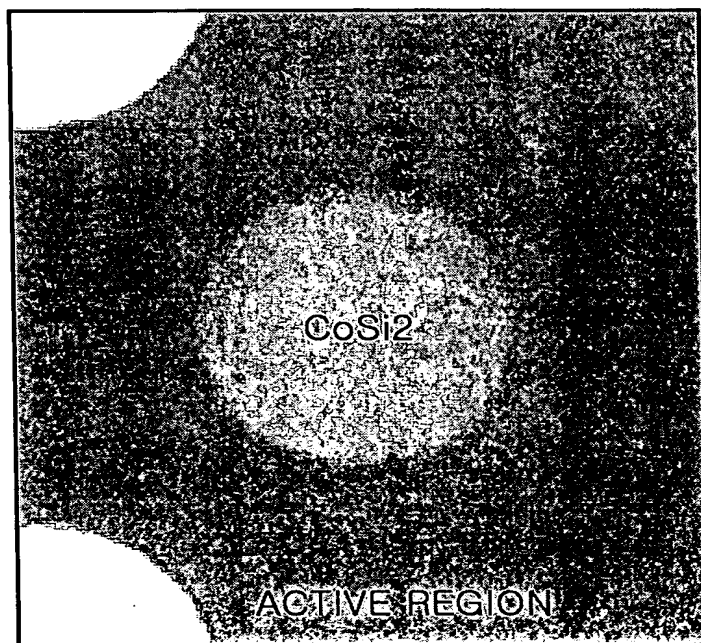


FIG. 9B



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FIG. 10A

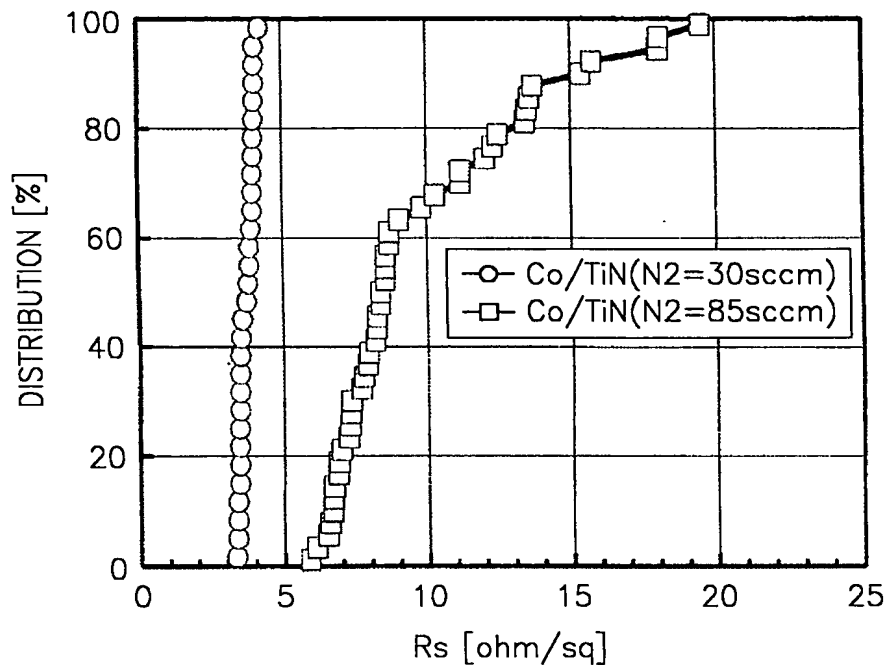


FIG. 10B

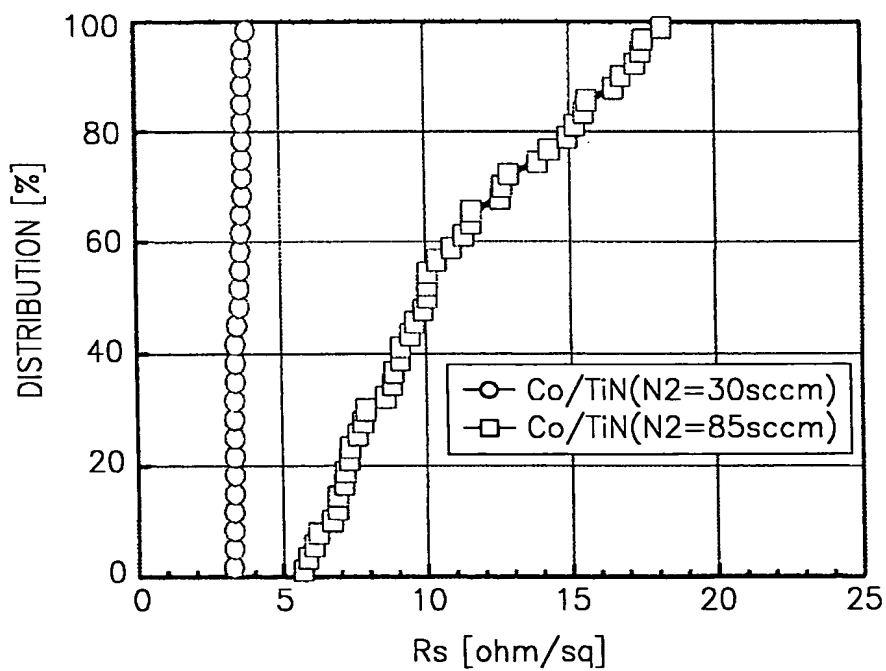
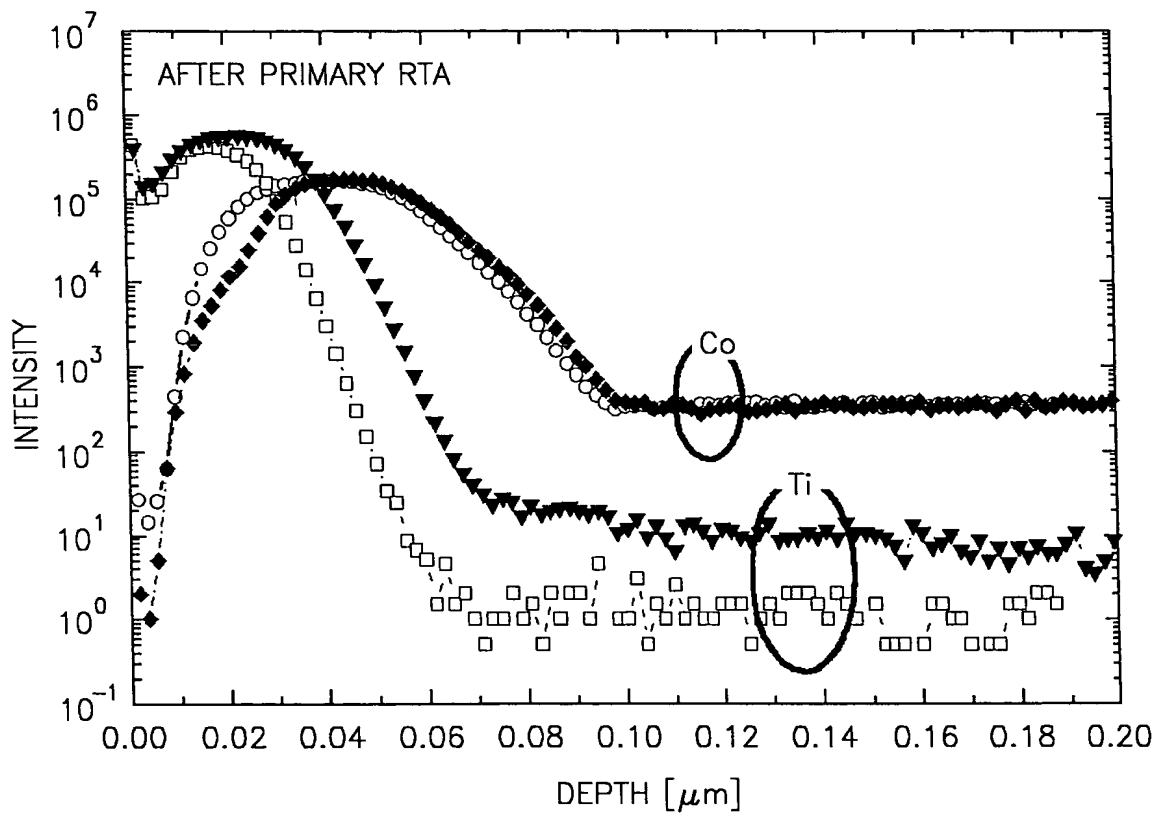


FIG. 11A



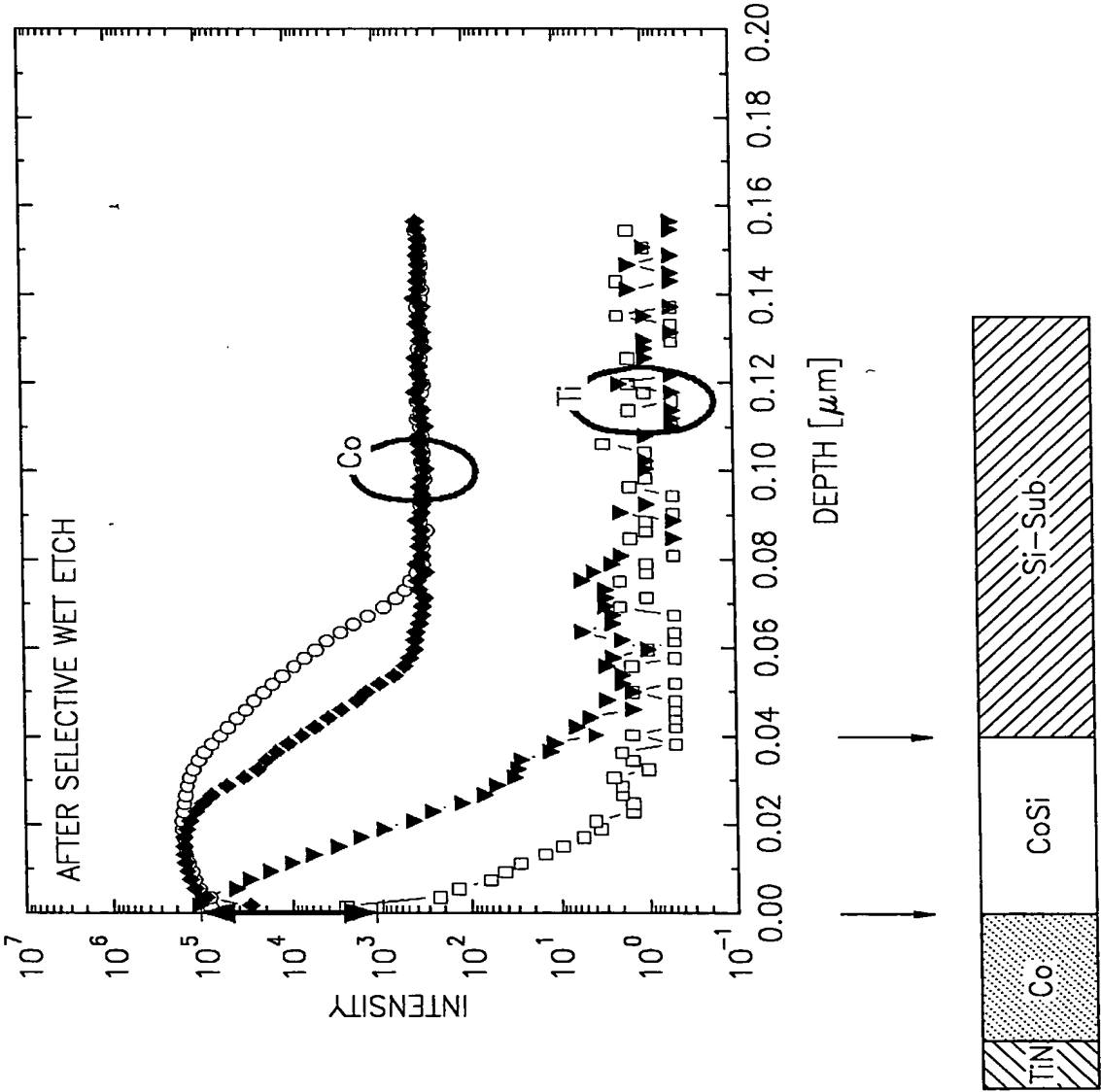


FIG. 12

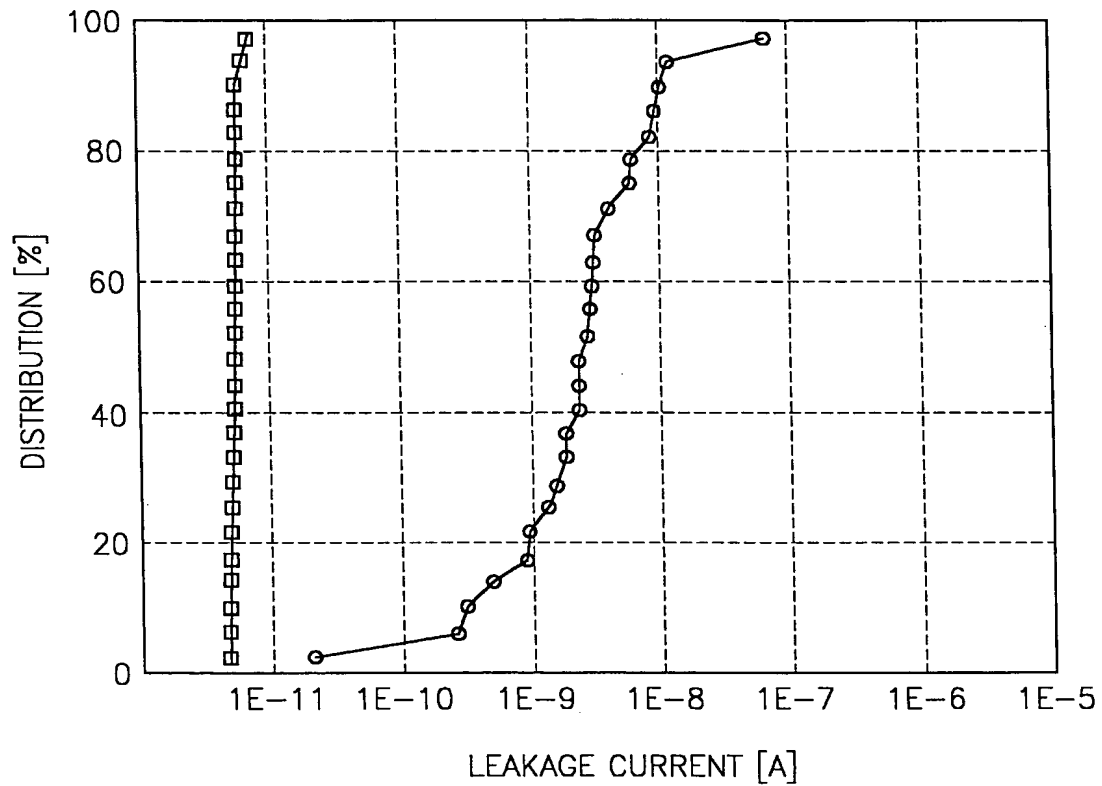


FIG. 13A

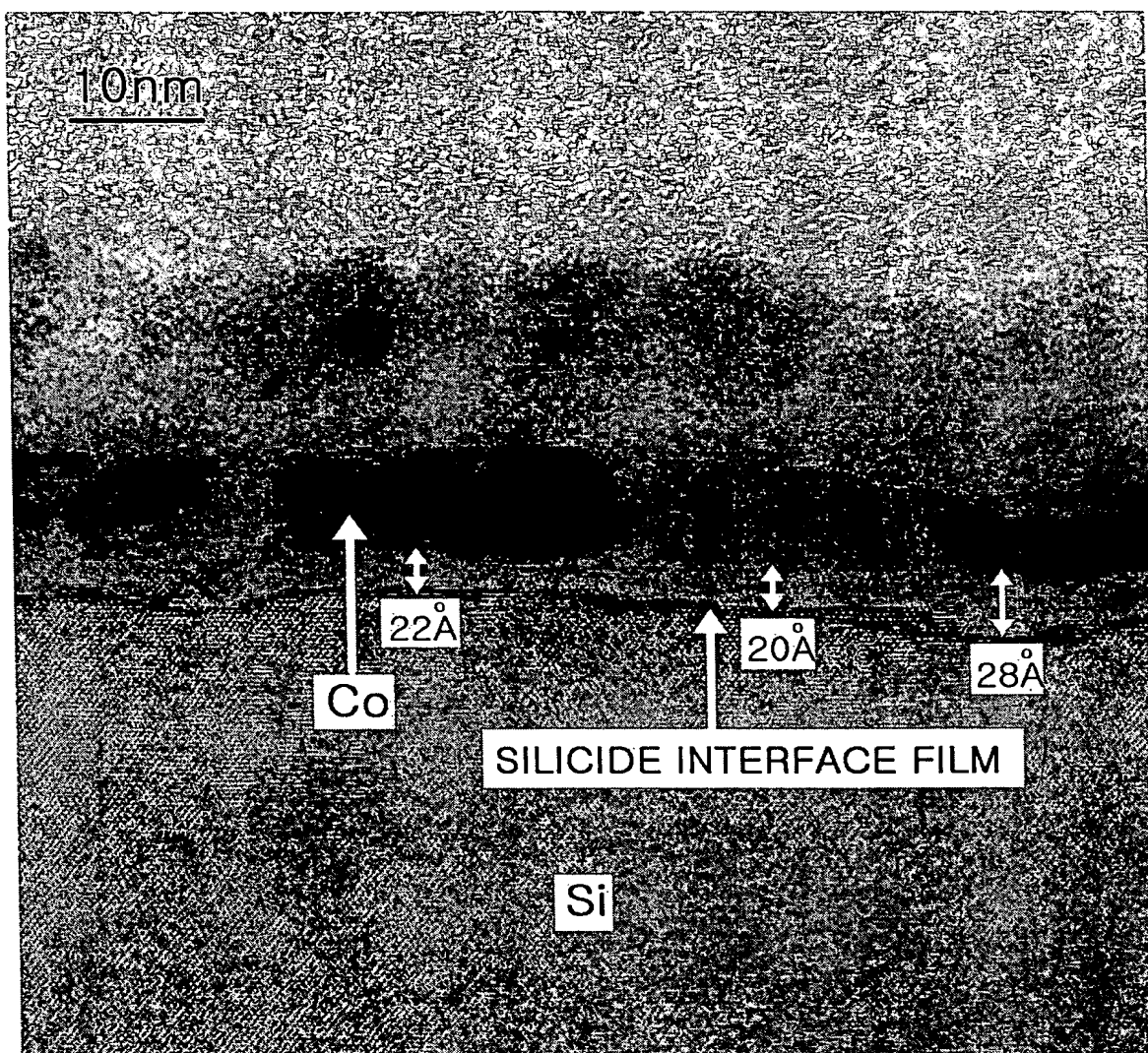


FIG. 13B

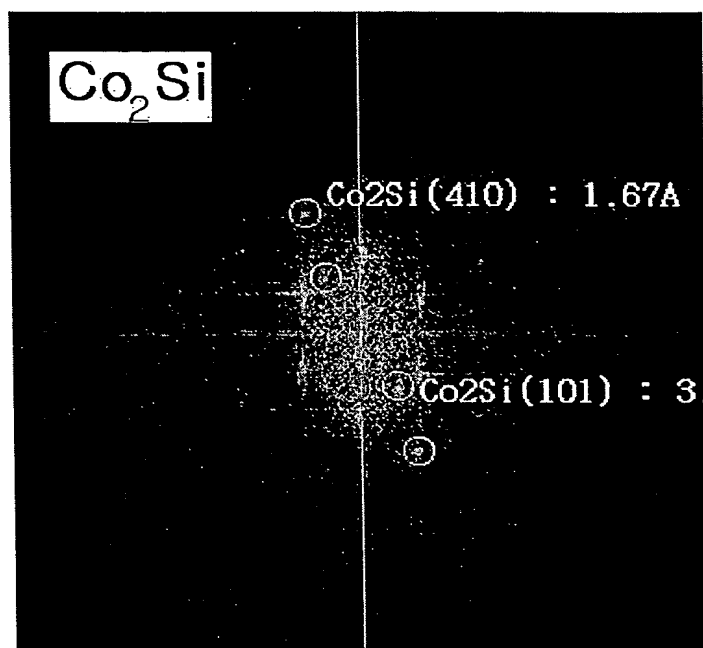


FIG. 13C

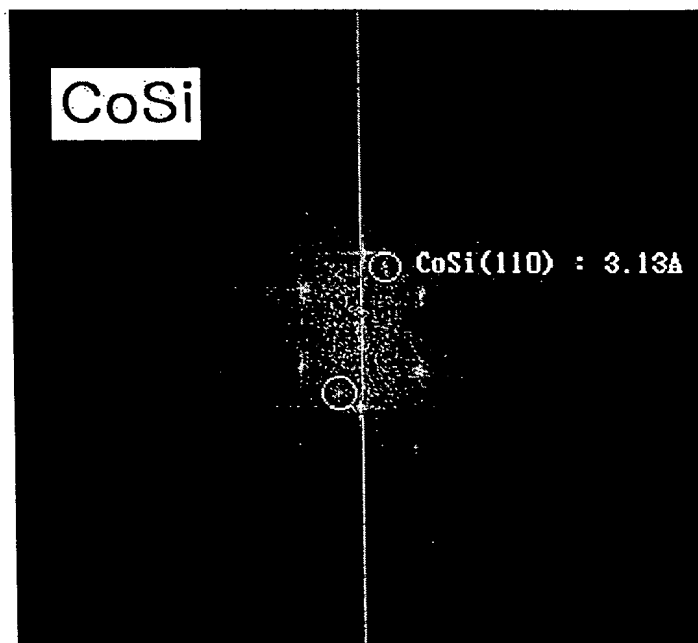


FIG. 14

